CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is:

1. A semiconductor structure comprising:

a semiconductor substrate containing silicon having an upper surface,

said substrate having at least one silicon-on-insulator region and at least one bulk semiconductor region adjacent said silicon-on-insulator region.

2. The semiconductor structure of claim 1 wherein said semiconductor substrate is selected from the group consisting of Si, SiGe and SiC.

3. The semiconductor structure of claim 1 wherein said silicon-on-insulator region includes a buried oxide region having continuous oxide from a first to a second side of said buried oxide region along a path generally parallel to a major surface of said substrate.

4. The semiconductor structure of claim 3 wherein said silicon-on-insulator region includes a buried oxide region having

first and second portions with an upper surface at corresponding first and second depths with respect to said upper surface of said semiconductor substrate to provide a silicon containing layer having corresponding portions with respective first and second thickness'.

5. The semiconductor structure of claim 4 wherein said first thickness is substantially equal to said first depth and said second thickness is substantially equal to said second depth.

6. The semiconductor structure of claim 4 wherein said first thickness is less than 1000 Å and said second thickness is greater than 1000 Å.

7. The semiconductor structure of claim 1 wherein said silicon-on-insulator region contains CMOS logic circuitry and said bulk semiconductor region contains DRAM circuitry.

8. The semiconductor structure of claim 1 wherein said silicon-on-insulator region contains a plurality of FET's and said bulk semiconductor region contains a plurality of trench capacitors.

9. The semiconductor structure of claim 3 wherein said silicon-on-insulator region includes a buried oxide region having

a first portion having an upper surface at said upper surface of said semiconductor substrate and a second portion with an upper surface at a first depth with respect to said upper surface of said semiconductor substrate to provide a silicon containing layer above said second portion having a first thickness.

10. The semiconductor structure of claim 1 further including a trench formed in said semiconductor substrate at the edge of said silicon-on-insulator region.

11. The semiconductor structure of claim 10 wherein said trench intersects an edge of said buried oxide region of said silicon-on-insulator region to remove a portion of the end of said buried oxide region.

12. The semiconductor structure of claim 7 further including a trench formed at the edge of said silicon-on-insulator region to intersect and remove crystalline defects.

13. The semiconductor structure of claim 7 further including a trench formed at the edge of said bulk semiconductor region to intersect and remove bulk semiconductor region crystalline defects.

14. The semiconductor structure of claim 12 further including a trench formed at the edge of said silicon-on-insulator region to intersect and remove silicon-on-insulator region and bulk semiconductor region crystalline defects.

15. The semiconductor structure of claim 12 wherein said trench includes sidewalls having a dielectric layer thereon.

16. The semiconductor structure of claim 15 wherein said dielectric layer includes silicon oxide and extends over a portion of said upper surface of said semiconductor substrate.

17. The semiconductor structure of claim 13 wherein said trench includes sidewalls having a dielectric layer thereon.

18. The semiconductor structure of claim 14 wherein said dielectric layer includes silicon oxide and extends over a portion of said upper surface of said semiconductor substrate.

19. The semiconductor structure of claim 17 wherein said dielectric layer includes silicon oxide and extends over a portion of said upper surface of said semiconductor substrate.

20. The semiconductor structure of claim 1 further including a trench formed through of said silicon-on-insulator region.

21. The semiconductor structure of claim 20 wherein said trench includes sidewalls having a dielectric layer thereon.

22. The semiconductor structure of claim 20 wherein said trench is filled with a material selected from the group consisting of p+ polysilicon, n+ polysilicon and a metal.

23. A semiconductor structure comprising:

a semiconductor substrate containing silicon and having an upper surface,

a trench formed in said upper surface having a first and second sidewall,

said first sidewall having a source and drain region spaced apart to define a channel therebetween, a dielectric layer over said channel region and a gate electrode over said dielectric layer to form a first field effect transistor on said first sidewall.

24. The semiconductor structure of claim 23 wherein said second sidewall includes a source and drain region spaced apart to define a channel there between, a dielectric layer over said channel region and a gate electrode over said dielectric layer to form a second field effect transistor on said second sidewall.

25. A semiconductor structure comprising:

a semiconductor substrate containing silicon and having an upper surface,

a trench formed in said upper surface having a first and second sidewall, and

a buried oxide layer formed below said upper surface and behind said first and second sidewalls,

said first sidewall having a source and drain region spaced apart to define a channel there between, a dielectric layer over said channel region and a gate electrode over said dielectric layer to form a first field effect transistor on said first sidewall.

26. The semiconductor structure of claim 25 wherein said second sidewall includes a source and drain region spaced apart to define a channel there between, a dielectric layer over said channel region and a gate electrode over said dielectric layer to form a second field effect transistor on said second sidewall.

27. A structure for forming electrical devices therein comprising:

a single crystal semiconductor substrate containing silicon having an upper surface, and

a plurality of spaced apart silicon-on-insulator regions having predetermined horizontal dimensions to provide a single crystal layer respectively over said buried oxide regions, each said buried oxide region having continuous oxide.

28. The structure of claim 27 wherein first and second portions of one of said buried oxide regions are at first and second respective depths below said upper surface to provide a single crystal silicon containing layer having respective first and second thickness'.

29. The structure of claim 27 wherein said buried oxide regions contain material selected from the group consisting of silicon precipitates and silicon islands.

30. A structure for forming electrical devices therein comprising:

a single crystal semiconductor substrate containing Si having an upper surface, and

a plurality of buried oxide regions formed therein by ion implantation of oxygen therein through openings in a patterned mask to provide a single crystal layer respectively over said buried oxide regions.

31. The structure of claim 30 wherein portions of one of said buried oxide regions are at respective depths below said upper surface to provide a single crystal layer thereover having a plurality of thickness'.

32. The structure of claim 30 wherein two of said buried oxide regions are at first and second respective depths below said upper surface to provide a single crystal layer thereover having first and second thickness'.

33. The structure of claim 31 wherein portions of one of said buried oxide regions are contiguous with oxide regions extending to said surface.

34. The structure of claim 31 further including at least one trench formed in said semiconductor substrate adjacent to one of said buried oxide regions.

35. A method for forming spaced apart silicon-on-insulator (SOI) regions on a silicon containing substrate comprising the steps of:

forming a first mask having openings therein on said silicon containing substrate,

implanting oxygen through said openings in said first mask into said substrate, and

annealing said substrate to form a plurality of first buried oxide regions below a silicon containing layer whereby said spaced apart silicon-on-insulator regions are formed.

36. The method of claim 35 wherein said step of implanting oxygen includes the step of selecting an ion energy to form said silicon containing layer having a thickness of less than 1000 Å.

37. The method of claim 35 wherein said step of implanting oxygen includes the step of selecting an ion energy to form said silicon containing layer having a thickness of at least 1000 Å.

38. The method of claim 35 wherein said step of forming a first mask includes the step of forming a mask having first regions therein of a first thickness to permit ions of oxygen to pass

there through into said substrate with reduced energy to form upon said step of annealing a plurality of second buried oxide regions.

39. The method of claim 38 wherein said step of forming a first mask includes the step of forming at least one of said first regions adjacent a respective opening to form upon said step of annealing a second buried oxide region contiguous with one of said plurality of first buried oxide regions.

40. The method of claim 35 further including the step of removing said first mask prior to said step of annealing.

41. The method of claim 35 wherein said step of forming a first mask includes the step of forming said first mask having first regions therein of a first material and of a first thickness to block substantially all ions from passing there through to provide at least one bulk semiconductor region free of oxygen implanted ions adjacent a silicon-on-insulator region.

42. The method of claim 35 wherein said step of forming a first mask includes the step of forming said first mask has a slanted edge at at least one of said openings at an angle with respect to an axis which is orthogonal to the surface of said silicon containing substrate and wherein during said step of implanting

ions pass through said slanted edge to provide said buried oxide region having a shaped edge.

43. The method of claim 42 wherein said angle of said slanted edge is in the range from 10 to 70 degrees.

44. The method of claim 35 wherein said step of implanting includes the step of implanting at an angle with respect to the surface of said silicon containing substrate.

45. The method of claim 44 wherein said step of implanting includes the step of implanting at an angle in the range from 10 to 90 degrees.

46. The method of claim 35 further including the step of forming a field effect transistor in said silicon containing layer.

47. The method of claim 35 further including the step of forming a trench in said silicon containing substrate at the edge of at least one of said silicon-on-insulator regions.

48. The method of claim 47 wherein said step of forming a trench includes the step of forming said trench to intersect an edge of said buried oxide region of said silicon-on-insulator region to remove a portion of the end of said buried oxide region.

49. The method of claim 35 further including the step of forming a trench in said silicon containing substrate through one of said silicon-on-insulator regions.

50. The method of claim 47 further including the step of filling said trench with a material selected from the group consisting of p+ polysilicon, n+ polysilicon and a metal.

51. A method for forming a structure for forming semiconductor circuits comprising the steps of:

selecting a semiconductor substrate containing silicon having a plurality of trenches therein,

forming a first mask on said substrate having an opening to expose a trench portion, and

implanting oxygen through openings in said first mask into said substrate and said trench portion, said step of implanting including the step of plasma immersion ion implantation of oxygen whereby oxygen ions pass through the sidewalls of said trench portion to form a buried oxide layer with respect to said sidewalls.

52. The method of claim 51 further including the step of forming a gate dielectric on the sidewalls of said trench.

53. The method of claim 51 further including the step of covering at least one trench portion with said first mask to prevent the formation of a buried oxide layer with respect to said sidewalls and bottom of said covered trench.

54. The method of claim 53 further including the step of forming a capacitor in said trench.

55. The method of claim 53 further including the step of forming an ohmic contact with the sidewalls and bottom of said covered trench.

56. The method of claim 52 further including the step of forming a gate electrode on said gate dielectric on said sidewalls in said trench.